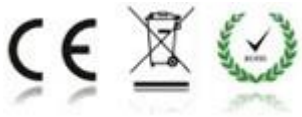
FES-QSFP28-100G/ER4-40km

FES-QSFP28

100Gb/s QSFP28 ER4 40km Optical Transceiver

- Hot pluggable FES-QSFP28 MSA form factor
- Compliant to Ethernet 100GBASE-ER4 40km
- Supports 103.1Gb/s aggregate bit rate
- Up to 30km reach for G.652 SMF without FEC
- Up to 40km reach for G.652 SMF with FEC
- Single +3.3V power supply
- Operating case temperature: 0~70oC
- Transmitter: cooled 4x25Gb/s LAN WDM EML TOSA (1295.56, 1300.05, 1304.58, 1309.14nm)
- Receiver: 4x25Gb/s APD ROSA
- 4x25G electrical interface (OIF CEI-28G
- Maximum power consumption 4.5W
- Duplex LC receptacle
- RoHS-6 compliant
- 

Applications

- 100GBASE-ER4 Ethernet Links
- Infiniband QDR and DDR interconnects
- Client-side 100G Telecom connections

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Description

This product is a 100Gb/s transceiver module designed for optical communication applications compliant to Ethernet 100GBASE-ER4 Lite standard. The module converts 4 input channels of 25Gb/s electrical data to 4 channels of LANWDM optical signals and then multiplexes them into a single channel for 100Gb/s optical transmission. Reversely on the receiver side, the module de-multiplexes a 100Gb/s optical input into 4 channels of LANWDM optical signals and then converts them to 4 output channels of electrical data.

The central wavelengths of the 4 LAN WDM channels are 1295.56, 1300.05, 1304.58 and 1309.14nm as members of the LANWDM wavelength grid defined in IEEE802.3ba.The high performance cooled LAN WDM EA-DFB transmitters and high sensitivity APD receivers provide superior performance for 100Gigabit Ethernet applications up to 30km links without FEC and 40km links with FEC.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP+ Multi-Source Agreement (MSA).It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

Functional Diagram

The transceiver module receives 4 channels of 25Gb/s electrical data, which are processed by a 4-channel Clock and Data Recovery (CDR) IC that reshapes and reduces the jitter of each electrical signal. Subsequently, EML laser driver IC converts each one of the 4 channels of electrical signals to an optical signal that is transmitted from one of the 4 cooled EML lasers which are packaged in the Transmitter Optical Sub-Assembly (TOSA). Each laser launches the optical signal in specific wavelength specified in IEEE802.3ba 100G BASE-ER4 requirements. These 4-lane optical signals will be optically multiplexed into a single fiber by a 4-to-1 optical WDMMUX. The optical output power of each channel is maintained constant by an automatic power control (APC) circuit. The transmitter output can be turned off by TX_DIS hardware signal and/or 2-wire serial interface.

The receiver receives 4-lane LANWDM optical signals. The optical signals are de-multiplexed by a 1-to-4 optical DEMUX and each of the resulting 4 channels of optical signals is fed into one of the 4 receivers that are packaged into the Receiver Optical Sub-Assembly (ROSA). Each receiver converts the optical signal to an electrical signal. The regenerated electrical signals are retimed and de-jittered and amplified by the RX portion of the 4-channel CDR. The retimed 4-lane output

electrical signals are compliant with CEI-28G-VSR interface requirements. In addition, each received optical signal is monitored by the DOM section. The monitored value is reported through the 2-wire serial interface. If one or more received optical signal is weaker than the threshold level, RX_LOS hardware alarm will be triggered.

A single +3.3V power supply is required to power up this product. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (includingthe2-wireserialinterface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. The ModSelL allows the use of this product on a single2-wireinterface bus – individual ModSelL lines must be used.

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP28 memory map.

The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

Low Power Mode (LPMode) pin is used to set the maximum power consumption for the product in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a “Low” state.

Interrupt (IntL) is an output pin. “Low” indicates a possible operational fault or a status critical tothehostsystem.Thehostidentifiesthesourceoftheinterruptusingthe2-wireserialinterface.TheIntLpin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

Transceiver Block Diagram

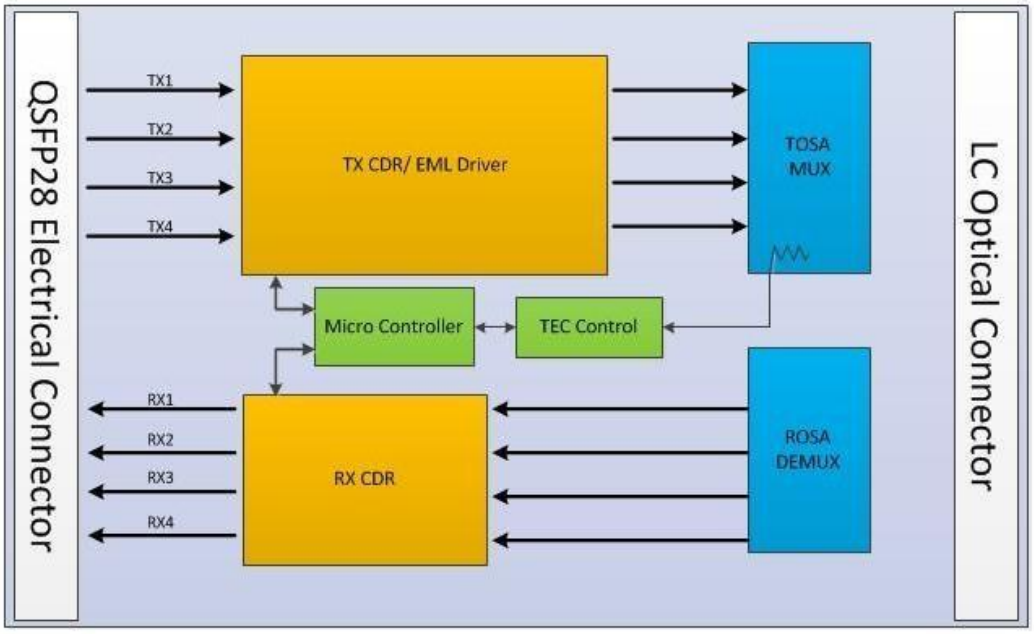


Figure 1. Transceiver Block Diagram

Pin Assignment and Description

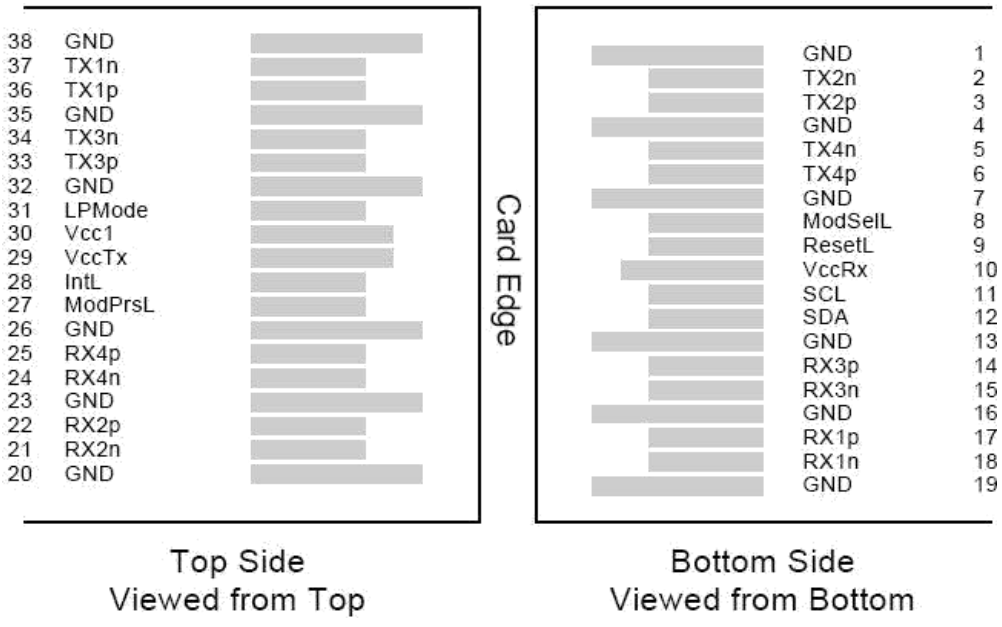


Figure 2. MSA compliant Connector

Pin Definition

PIN	Logic	Symbol	Name/Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Output	

35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

Notes:

1、GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

2 、 VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown in Figure3 below. VccRx, Vcc1 and VccTx may be internally connected within the module in any combination. The connector pins are each rated for a maximum current of 1000mA.

Recommended Power Supply Filter

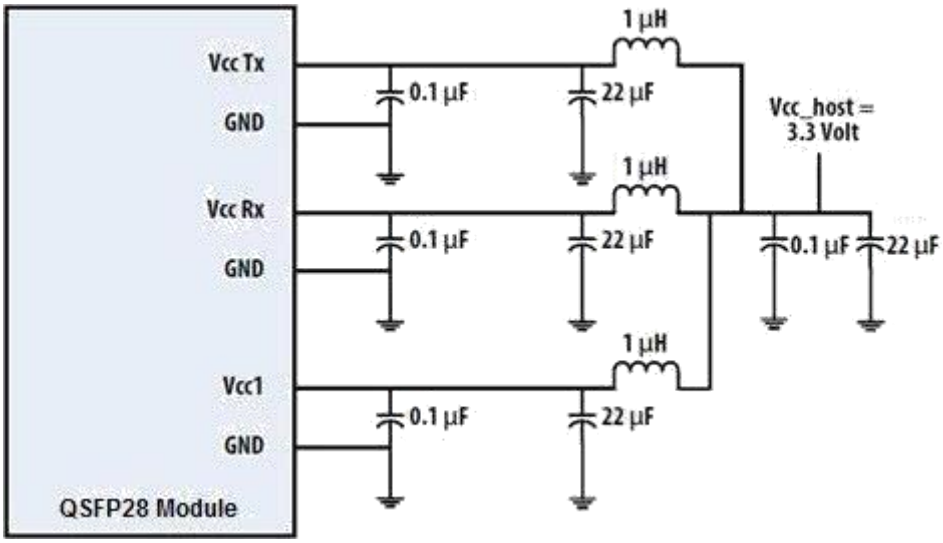


Figure 3. Recommended Power Supply Filter

Absolute Maximum Ratings

1. Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T_S	-40	85	degC	
Operating Case Temperature	T_{OP}	0	70	degC	
Power Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	0	85	%	
Damage Threshold, each Lane	TH_d	-3.0		dBm	

Recommended Operating Conditions and

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating Case Temperature	T_{OP}	0		70	degC	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Data Rate, each Lane			25.78125		Gb/s	
Data Rate Accuracy		-100		100	ppm	
Control Input Voltage High		2		Vcc	V	
Control Input Voltage Low		0		0.8	V	
Link Distance with G.652 (without	D1			30	km	1
Link Distance with G.652 (with FEC)	D2			40	km	1

Notes:

1. Depending on actual fiber loss/km (link distance specified is for fiber insertion loss of0.4dB/km)

Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Test Poin	Min	Typical	Max	Units	Notes
Power Consumption				4.5	W	
Supply Current	Icc			1.36	A	
Transmitter(each Lane)						
Overload Differential Voltage pk-pk	TP1a	900			mV	
Common Mode Voltage (Vcm)	TP1	-350		2850	mV	1
Differential Termination	TP1			10	%	At1MHz
Differential Return Loss (SDD11)	TP1			SeeCEI-28G-VSR	dB	
Common Mode to Differential conversion and Differential to Common	TP1			SeeCEI-28G-VSR	dB	
Stressed Input Test	TP1a	SeeCEI-28G-VSR				
Receiver (each Lane)						
Differential Voltage, pk-pk	TP4			900	mV	
Common Mode Voltage (Vcm)	TP4	-350		2850	mV	1
Common Mode Noise, RMS	TP4			17.5	mV	
Differential Termination	TP4			10	%	At1MHz
Differential Return Loss (SDD22)	TP4			SeeCEI-28G-VSR	dB	

Common Mode to Differential conversion and Differential to Common Mode	TP4			SeeCEI-28G-VSR	dB	
Common Mode Return Loss (SCC22)	TP4			-2	dB	2
Transition Time, 20 to80%	TP4	9.5			ps	
Vertical Eye Closure(VEC)	TP4			5.5	dB	
Eye Width at 10^{-15}probability(EW15)	TP4	0.57			UI	
Eye Height at 10^{-15}probability(EH15)	TP4	228			mV	

Notes:

2. Vcm is generated by the host. Specification includes effects of ground offset voltage.
3. From 250MHz to30GHz.

Optical Characteristics

Ethernet 100GBASE-ER4Lite						
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Units**	**Notes**
Lane Wavelength	L0	1294.53	1295.56	1296.59	nm	
	L1	1299.02	1300.05	1301.09	nm	
	L2	1303.54	1304.58	1305.63	nm	
	L3	1308.09	1309.14	1310.19	nm	
Transmitter						
SMSR	SMSR	30			dB	
Total Average Launch Power	P_T			10.5	dBm	
Average Launch Power, each Lane	P_{AVG}	-2.9		4.5	dBm	1
OMA, each Lane	P_{OMA}	0.1		4.5	dBm	2
Difference in Launch Power between any Two	Ptx, diff			3.6	dB	
Launch Power in OMA minus Transmitter and Dispersion Penalty(TDP), each Lane		-0.65			dBm	
TDP, each Lane	TDP			2.5	dB	
Extinction Ratio	ER	7			dB	

$RIN_{20}OMA$	RIN			-130	dB/Hz	
Optical Return Loss Tolerance	TOL			20	dB	
Transmitter Reflectance	R_T			-12	dB	
Average Launch Power OFF Transmitter, each	Poff			-30	dBm	
Eye Mask{X1, X2, X3, Y1, Y2,Y3}		{0.25, 0.4, 0.45, 0.25, 0.28,0.4}				
Receiver						
Damage Threshold, each Lane	TH_d	-3.0			dBm	3
Average Receive Power, each		-16.9		-4.9	dBm	for 30km
						Link Distanc
Average Receive Power, each		-20.9		-4.9	dBm	for 40kmLi nkDista
Receive Power (OMA), each Lane				-1.9	dBm	
Receiver Sensitivity (OMA),each Lane	SEN1			-14.65	dBm	For BER $=1x10^{-12}$
Stressed Receiver Sensitivity(OMA), each				-12.65	dBm	For BER $=1x10^{-12}$
Receiver Sensitivity (OMA),each Lane	SEN2			-18.65	dBm	For BER $=5x10^{-5}$
Stressed Receiver Sensitivity(OMA), each				-16.65	dBm	For BER $=5x10^{-5}$
Receiver reflectance				-26	dB	
Difference in Receive Power between any Two Lanes(Average and OMA)	Prx, diff			3.6	dB	
LOS Assert	LOSA		-26		dBm	
LOS Deassert	LOSD		-24		dBm	
LOS Hysteresis	LOSH	0.5			dB	
Receiver Electrical 3 dB upper Cutoff Frequency,	Fc			31	GHz	
Conditions of Stress Receiver Sensitivity Test (Note4)						
Vertical Eye Closure Penalty, each Lane			1.5		dB	
Stressed Eye J2 Jitter, each Lane			0.3		UI	
Stressed Eye J9 Jitter, each Lane			0.47		UI	

Notes:

1、The minimum average launch power spec is based on ER not exceeding 9.5dB and transmitter OMA

higher than0.1dBm.

2、Even if the TDP < 0.75 dB, the OMA min must exceed the minimum value specified here.

3、The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

4 、 Vertical eye closure penalty, stressed eye J2 jitter, and stressed eye J9 jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Digital Diagnostic Functions

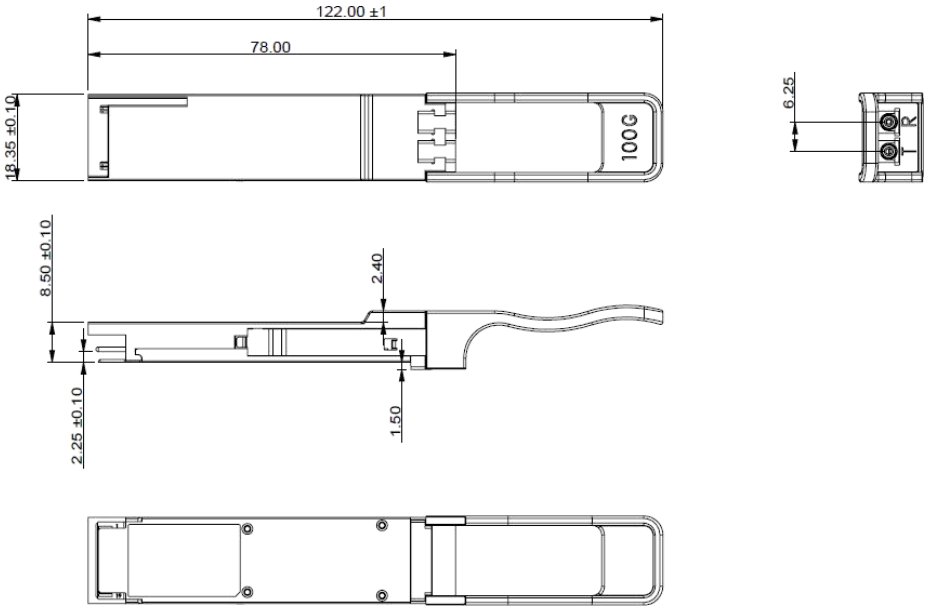
The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Ma	Unit	Notes
Temperature monitor absolute error	DMI_Temp	-3	+3	deg C	Over operating temperature range
Supply voltage monitor absolute error	DMI_VCC	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	1
Channel Bias current monitor	DMI_Ibias_C	-10	10	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	1

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1dB fluctuation, or a +/- 3 dB total accuracy.

Mechanicl Dimensions



ESD

Thistransceiver is specified as ESD threshold 1kV for SFI pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Laser Safety

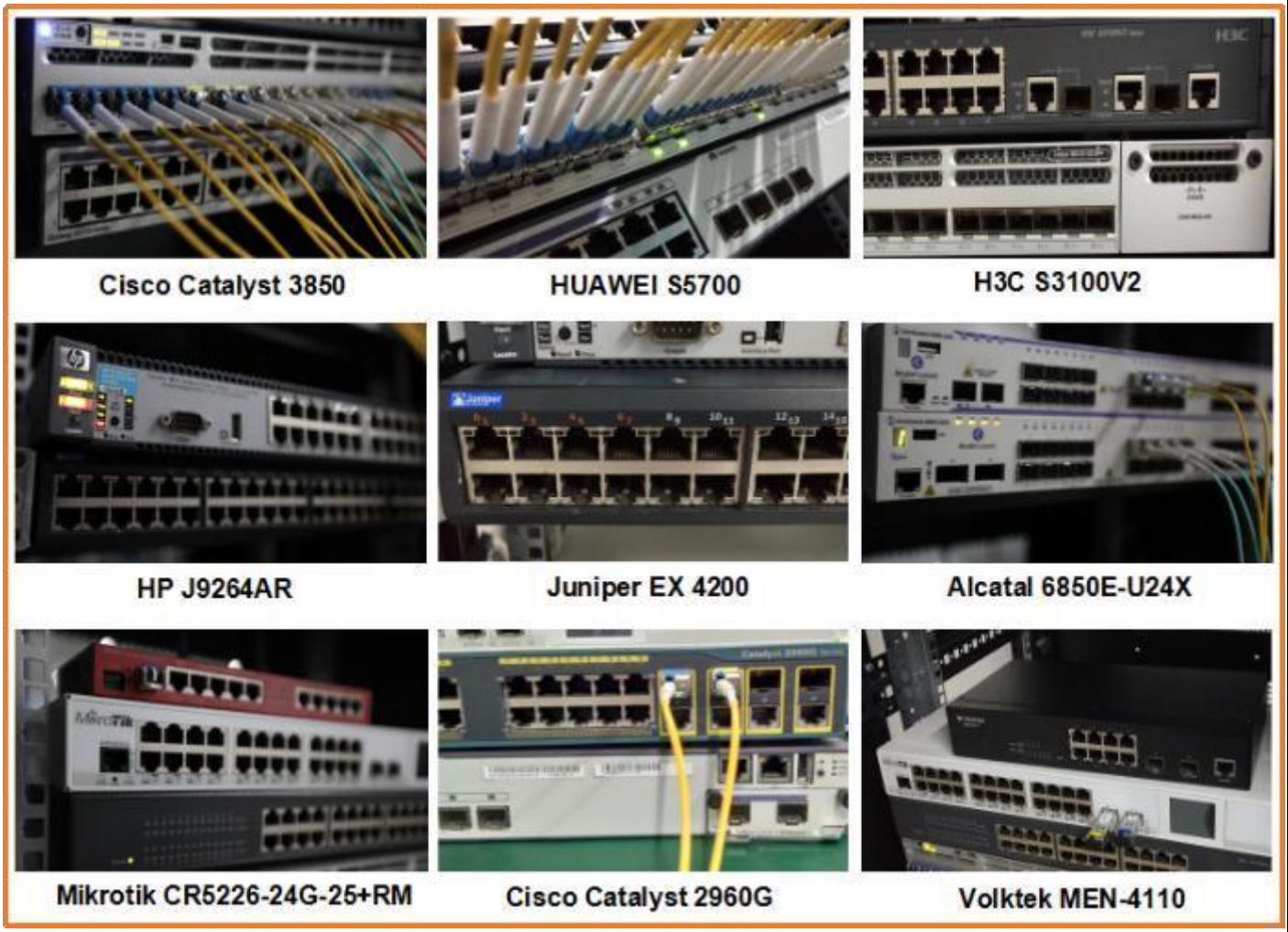
This is a Class1 Laser Product according to EN60825-1:2014. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24,2007).

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Compatibility Test

In order to ensure the product compatibility, our products will be tested on the switch before shipment. Our modules can compatible with many mainstream brand switches, such as Cisco, Juniper, Extreme, Brocade, IBM, H3C, HP, Huawei, D-Link, Mikrotik, ZTE, TP-Link...

Our test equipment: VOLKTEK MEN-4110, HP 2530-8G, CRS226-24G-25+RM, Catalyst 2960G Series, Catalyst 3850 XS 10G SFP+, Catalyst 3750-E Series, HUAWEI S5700Series, H3C S3100V2 Series, Juniper-EX4200, etc.



Product Production Process

Quality Assurance

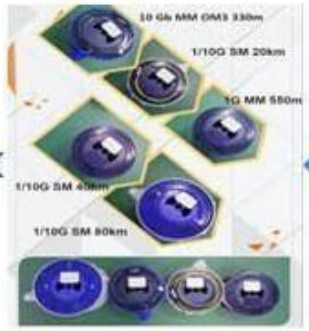
Continuous introduction of new equipment, produced by strict standards, strict quality inspection, to guarantee the high quality standard of each product.

Standardized Production Line

Professional Welding

Assembling

Cleaning end face



Distance Testing

Aging Testing

Product Initial Test

Switch Testing

Product Final Test